

Transient thermal analysis model creation method for semiconductor devices

- DSRC model creation method -

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KEY WORDS: common infrastructure, computer aided engineering, modeling, Transient Thermal Analysis (F2)

The development period of automobile parts is required to be shortened year by year, and the need for heat transfer analysis in design is increasing to achieve this. In recent years, not only heat transfer analysis in steady state but also transient thermal analysis is required according to the operation of the circuit. In order to correspond to transient thermal analysis, two models such as a DSRC model using a data sheet and a DNRC model using measured values, expressing transient thermal resistance characteristics in a thermal network have been proposed so far. In this report, we show the know-how and procedures for creating the DSRC model, and the influence of the semiconductor element mounting environment at the time of model creation and the influence of the model topology on the analysis accuracy.

The creation of the DSRC model is roughly divided into three stages. First, the environment acquired the transient heat resistance characteristic on the data sheet is reproduced by the heat transfer analysis model. Next, fitting heat resistance and heat capacity and finally evaluate the accuracy of the model. The transient thermal resistance characteristic is generally described in the data sheet, such as a thermal resistance (θ_{ja}) between the junction and the surrounding environment and its (θ_{jc}) between the junction and the semiconductor element surface (case). However, it is not uniform. In addition, the position of the case is not basically described, and varies depending on the manufacturer and model number. Furthermore, it is uncertain whether or not the environment in which the transient thermal resistance characteristics are measured is described in the data sheet because it is carried out by each company's own method. Therefore, we evaluated how the mounting environment of semiconductor devices affects the model accuracy.

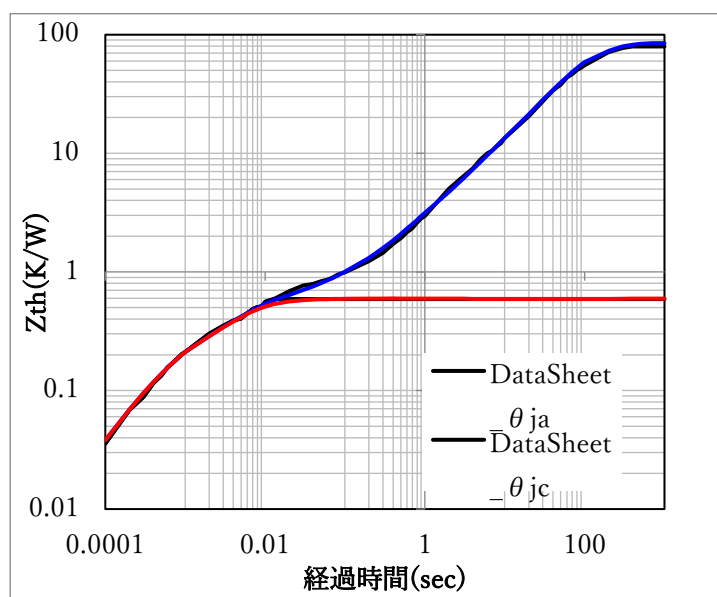


Fig. 1 Comparison of transient thermal resistance characteristics

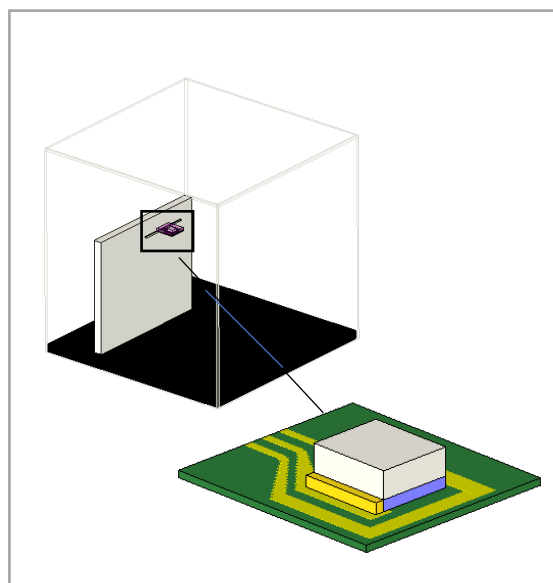


Fig.2 JESD 51-2A mounting environment